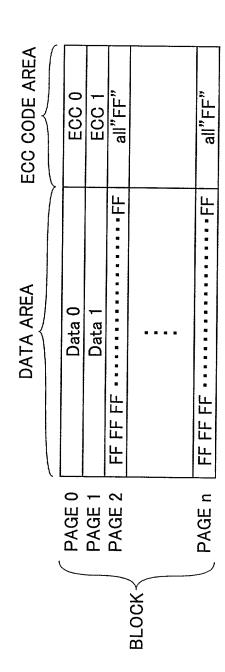
r<sub>Y</sub>

FIG.1



MEMORY CELL ARRAY ECC-GENERATION
-&ERROR-CORRECTION
CIRCUIT **FIG.2** 13a 12 DATA BUFFER (512 BYTES) ECC SUSPENSION 14 DATA BUFFER (3 BYTES) BUFFER-CONTROL CIRCUIT CIRCUIT <u>ლ</u> CONTROL SIGNAL AND DATA I/O

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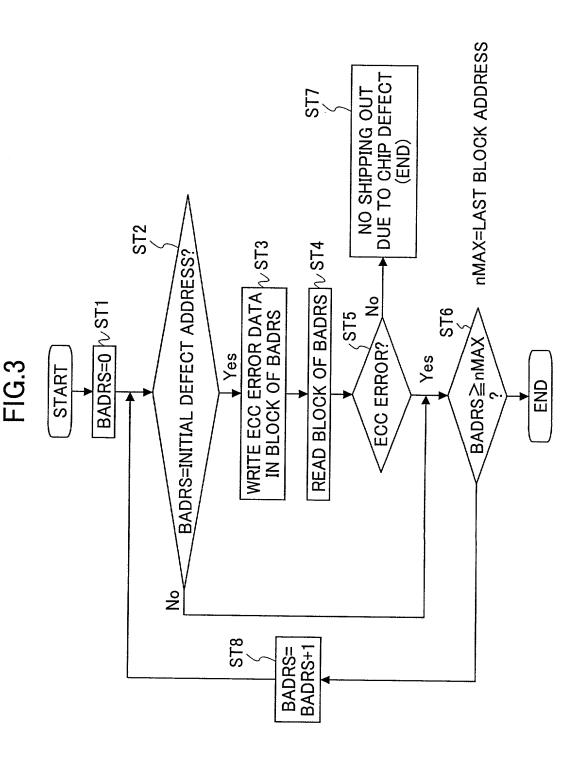


FIG 4

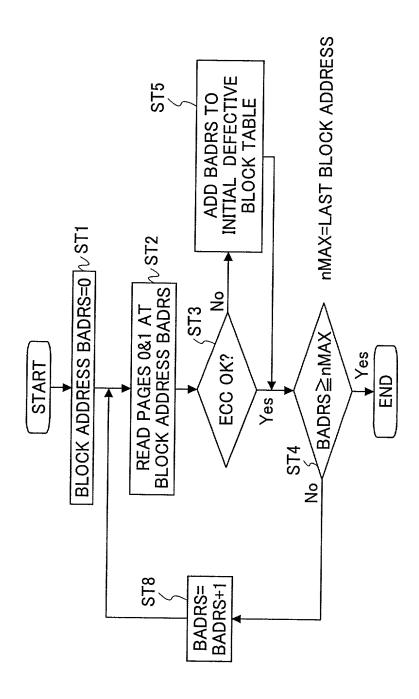


FIG.5

ECC CODE AREA (3 BYTES)	00 00 00	00 00 00	all"FF"		all"FF"
DATA AREA (512 BYTES)	FF FF FFFF	FF FF         FF	FF FF FF	• • •	보는 무슨 무슨
	PAGE 0	PAGE 1	PAGE 2		/ PAGE n
				BLOCK	

## FIG. 6

TATUS DESCRIPTION	NS=0	ON=0	I/O2 ECC ERROR CORRECTION 0=NO DATA CORRECTION, 1=DATA CORRECTED	R CORRECTION RESERVED	R CORRECTION RESERVED	R CORRECTION RESERVED	DY/BUSY 0=BUSY, 1=READY	
STATUS	PROGRAM/ERASE	I/O1 ECC ERROR DETECTION	<b>ECC ERROR CORRECTION 0=</b>	I/03 ECC ERROR CORRECTION	I/O4 ECC ERROR CORRECTION	I/O5 ECC ERROR CORRECTION	READY/BUSY	
	00/1	1/01	1/02	1/03	1/04	1/05	90/I	

FIG. 7

